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LM21/1202

EXAMINER	
BUTLER, D	
ART UNIT	PAPER NUMBER
2787	4

12/02/97

DATE MAILED:

This is a communication from the examiner in charge of your application.  
COMMISSIONER OF PATENTS AND TRADEMARKS

☒ This application has been examined ☒ Responsive to communication filed on 9-4-96 ☐ This action is made final.

A shortened statutory period for response to this action is set to expire 3 month(s), \_\_\_\_\_ days from the date of this letter.  
Failure to respond within the period for response will cause the application to become abandoned. 35 U.S.C. 133

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

- |   |  |
|---|--|
| 1. <input checked="" type="checkbox"/> Notice of References Cited by Examiner, PTO-892. | 2. <input checked="" type="checkbox"/> Notice of Draftsman's Patent Drawing Review, PTO-948. |
| 3. <input checked="" type="checkbox"/> Notice of Art Cited by Applicant, PTO-1449.      | 4. <input type="checkbox"/> Notice of Informal Patent Application, PTO-152.                  |
| 5. <input type="checkbox"/> Information on How to Effect Drawing Changes, PTO-1474.     | 6. <input type="checkbox"/> _____  |

Part II SUMMARY OF ACTION

1. ☒ Claims 1-20 are pending in the application.

Of the above, claims \_\_\_\_\_ are withdrawn from consideration.

2. ☐ Claims \_\_\_\_\_ have been cancelled.

3. ☐ Claims \_\_\_\_\_ are allowed.

4. ☒ Claims 1-20 are rejected.

5. ☐ Claims \_\_\_\_\_ are objected to.

6. ☐ Claims \_\_\_\_\_ are subject to restriction or election requirement.

7. ☐ This application has been filed with informal drawings under 37 C.F.R. 1.85 which are acceptable for examination purposes.

8. ☐ Formal drawings are required in response to this Office action.

9. ☐ The corrected or substitute drawings have been received on \_\_\_\_\_. Under 37 C.F.R. 1.84 these drawings are ☐ acceptable; ☐ not acceptable (see explanation or Notice of Draftsman's Patent Drawing Review, PTO-948).

10. ☐ The proposed additional or substitute sheet(s) of drawings, filed on \_\_\_\_\_, has (have) been ☐ approved by the examiner; ☐ disapproved by the examiner (see explanation).

11. ☐ The proposed drawing correction, filed \_\_\_\_\_, has been ☐ approved; ☐ disapproved (see explanation).

12. ☐ Acknowledgement is made of the claim for priority under 35 U.S.C. 119. The certified copy has ☐ been received ☐ not been received ☐ been filed in parent application, serial no. \_\_\_\_\_; filed on \_\_\_\_\_.

13. ☐ Since this application appears to be in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under Ex parte Quayle, 1935 C.D. 11; 453 O.G. 213.

14. ☐ Other

EXAMINER'S ACTION

1. This action is in response to the application filed on November 4, 1996. Claims 1-20 are pending.
2. Effective November 16, 1997, the Examiner handling this application will be assigned to a new Art Unit as a result of the consolidation into Technology Center 2700. See the forth coming Official Gazette notice dated November 11, 1997. For any written or facsimile communication submitted ON OR AFTER November 16, 1997, this Examiner, who was assigned to Art Unit 2316, will be assigned to Art Unit 2787. Please include the new Art Unit in the caption or heading of any communication submitted after the November 16, 1997 date. Your cooperation in this matter will assist in the timely processing of the submission and is appreciated by the Office.
3. Claims 5-6, 8-9, 11 and 14-20 are rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claims 5, 11 and 14, these claims recite desired functional results without reciting any structural elements capable of performing the purported functions. Therefore, the claims are unclear as to what performs the recited functions.

Regarding claims 6, 8-9 and 17, the phrases "said output frequencies", "said inputs to said multiplexer" and "the impedance" lack proper antecedent basis. In addition, claims 8 and 9 are unclear as to the relationship between the internally and externally generated clocks and the structural elements recited in claim 1. What are the clocks internal and external to?

Regarding claim 15, the claim is unclear as to the relationship between the steps recited in the body of the claim and the structural elements recited in the preamble. Particularly, it is unclear as to whether the recited steps provide an integrated programmable circuit and a clock generation circuit as claimed.

Claim 16 is rejected because it incorporates deficiencies of claim 15.

Regarding claims 18-20, the claims are unclear as to the relationship between the internally and externally generated clocks and the structural elements recited in claim 15. What are the clocks internal and external to?

4. The following art rejections of claims 5-6, 8-9, 11 and 14-20 are according to the examiner's understanding of the claimed invention in spite of the above 35 USC 112, second paragraph rejections.
5. The following is a quotation of the appropriate paragraphs of 35 USC § 102 that form the basis for the rejections under this section made in this Office action:  
  
A person shall be entitled to a patent unless --  
  
(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.  
  
(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.
6. This application currently names joint inventors. In considering patentability of the claims under 35 USC 103, the examiner presumes that the subject matter of the various claims

was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of potential 35 USC 102(f) or (g) prior art under 35 USC 103.

7. The following is a quotation of 35 USC 103 which forms the basis for all obviousness rejections set forth in this Office action:

A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Subject matter developed by another person, which qualifies as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

8. Claims 1-4, 6-7, 12-13 and 15-16 are rejected under 35 USC 102(b) as being anticipated by Davis et al., U.S. Patent 4,893,271.

Per claims 1, 12 and 15:

A) Davis et al teach the following claimed items:

1. means/first circuit for storing programmable information with Frequency Control Register 240 or RAM 252 or ROM 250 of figure 3 and at column 7, lines 41-55;
2. means/second circuit for (capable of) providing a plurality of output clocks in response to a reference clock frequency with Frequency Synthesized Timing Generator 200 of figures 2, 3 and 4 and at column 9, lines 7-43.

Per claims 2, 13 and 16:

Davis et al teach providing a plurality of output clocks which are individually programmable to a plurality of frequencies at column 9, lines 33-55.

Per claim 3:

See the rejection of claim 1.

Per claim 4:

Davis et al teach the output clock being accessible through one or more input/output pins with pins 110 and/or 112 and/or 114 of figures 2 and 3 and at column 5, line 56 - column 6, line 2.

Per claim 6:

See the rejection of claim 1.

Per claim 7:

Davis et al teach the reference clock comprising one or more clock frequencies with the reference clock output on line 202 of figures 2, 3 and 4.

9. Claims 5, 10-11, 14 and 17-20 are rejected under 35 USC 103 as being unpatentable over Davis et al., U.S. Patent 4,893,271, in view of Hotta et al., U.S. Patent 5,506,982.

Per claims 5, 11, 14 and 17:

Claims 5, 11 and 14 recite desired functional results without reciting any structural elements capable of performing the purported functions. Therefore, these recited functions are not deemed to carry any patentable weight. In addition, the recited functions are well known in the timing art and would have been obvious to one of ordinary skill in

the art.

Per claim 10:

Davis et al teach the claimed elements as described above in the rejection of claim 1. The claim seems to differ from Davis et al in that Davis et al fails to explicitly teach providing a programmable logic device comprising the elements of claim 1 as claimed. However, Hotta teaches that it is known to provide a programmable logic device comprising the elements of claim 1 as set forth with figures 1, 8 and 16, at column 9, lines 22-50 and at column 11, lines 13-39. It would have been obvious to one having ordinary skill in the data processing art at the time the invention was made to provide a programmable logic device comprising the elements of claim 1, as taught by Hotta, in order to provide a PLA which is controlled by a phase locked two phase clock signal. One of ordinary skill in the art would have been motivated to combine Davis and Hotta because of Hotta's suggestion at column 1, lines 22-30, at column 5, lines 4-23, at column 9, lines 46-50 and with figures 1, 8, 16 and 23. It would have been obvious for one of ordinary skill in the art to combine Davis and Hotta because they are both directed to the problem of generating a plurality of phase locked clock signals for a programmable logic device.

Per claims 18-20:

Claims 18-20 recite obvious variations of well known clock signal generation procedures and would have been obvious to one of ordinary skill in the art.

10. Claims 1, 10, 12 and 15 are rejected under 35 USC 102(e) as being anticipated by Hotta et al., U.S. Patent 5,506,982.

Per claims 1, 12 and 15:

A) Hotta et al teach the following claimed items:

1. means/first circuit for storing programmable information with Memory 2900 or figure 29 and/or Memory 3407 of figure 34;
2. means/second circuit for (capable of) providing a plurality of output clocks in response to a reference clock frequency with figures 1 and 16 and at column 9, lines 22-50 and at column 11, lines 13-39.

Per claim 10:

Hotta teaches that it is known to provide a programmable logic device comprising the elements of claim 1 as set forth with figures 1, 8 and 16, at column 9, lines 22-50 and at column 11, lines 13-39.

11. Claims 8 and 9 are so unclear as to their meaning and their relationship to claims 1 and 7 that the examiner can not apply art to these claims.
12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis M. Butler whose telephone number is (703) 305-9663. The examiner can normally be reached on Monday-Friday from 9:30 AM to 6:00 PM.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Dennis M. Butler  
November 24, 1997

*Dennis M. Butler*  
Dennis M. Butler  
Primary Examiner  
Group 2700